

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (Currently Amended): A liquid crystal display panel comprising: first and second substrates;

a photo-hardening sealant between the first and second substrates;

a plurality of gate lines in an active region;

a plurality of gate pads in a first pad region;

a plurality of data lines arranged to cross the gate lines;

a plurality of data pads in a second pad region

a plurality of pad links connecting the gate lines and the gate pads, and the data lines and the data pads, a plurality of metal lines on the first substrate, wherein the plurality of pad links metal lines
are formed of a transparent conductive film at least at portions where the metal lines cross one another; and

a liquid crystal layer between the first and second substrates.

Claims 2-3 (Cancelled).

Claim 4 (Currently Amended): The panel of claim 1 [[3]], wherein ~~at least a portion of the pad links of the gate lines and the gate pads~~ are [[is]] formed of the transparent conductive film.

Claim 5 (Currently Amended): The panel of claim 1 [[3]], wherein ~~at least a portion of the pad links of the data lines and the data pads~~ are [[is]] formed of the transparent conductive

Claims 6-25 (Canceled).

Claim 26 (New): The panel of claim 1, wherein the transparent conductive film includes indium tin oxide (ITO).

Claim 27 (New): A liquid crystal display panel comprising:

a first substrate;

a second substrate having an active region and a pad region thereon;

a photo-hardening sealant along a boundary between the active region and the pad region;

a plurality of pads formed in the pad region;

a plurality of lines arranged to cross one another in the active region;

a plurality of pad links formed of a transparent conductive film connecting the pads and the lines;

and

a liquid crystal layer between the first and second substrates.

Claim 28 (New): The panel of claim 27, wherein the transparent conductive film includes ITO.

Claim 29 (New): The panel of claim 27, wherein the pads include a plurality of gate pads each for receiving a gate driving signal from an external driving IC applied thereto and a plurality of data pads each for receiving a data signal from the external driving IC applied thereto.

Claim 30 (New): The panel of claim 29, further comprising a gate insulating film on the gate pads and the data pads.

Claim 31 (New): The panel of claim 27, wherein the pad links include a gate pad link connecting the gate pad and a gate line, and a data pad link connecting the data pad and a data line.

Claim 32 (New): The panel of claim 27, wherein the pad links include a plurality of gate pad links connected to a plurality of gate lines and a plurality of data pad links connected to a plurality of data lines.

Claim 33 (New): The panel of claim 27, wherein the lines include a plurality of gate lines and a plurality of data lines, the gate lines and the data lines crossing one another, thereby defining a plurality of pixel regions.

Claim 34 (New): The panel of claim 33, further comprising a thin film transistor at a crossing of the gate and data lines.

Claim 35 (New): The panel of claim 33, wherein the pixel regions include a pixel electrode.